

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address.

Respectfully submitted,



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TI-25856-9601-0001

Version With Markings To Show Changes Made

In the specification:

The following paragraph has been inserted at page 1, before line 1:

--This application claims priority under 35 USC § 119(e)(1) of provisional application number 60/258,607 filed 12/28/00.--

TI-25856 Page 3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

James D. Huffman *et al.*

Serial No.: TBD

Filed: Herewith

For: Memory Architecture for Micromirror Cell

Docket No.: TI-25856

Art Unit: TBD

Examiner: TBD

LETTER TO OFFICIAL DRAFTSPERSON

December 20, 2001

Assistant Commissioner for Patents
Washington, D.C. 20231

Draftsperson:

Applicants submit formal drawings (7 sheets) for the above-identified application.
Please charge any necessary fees to the deposit account of Texas Instruments
Incorporated, Account No. 20-0668.

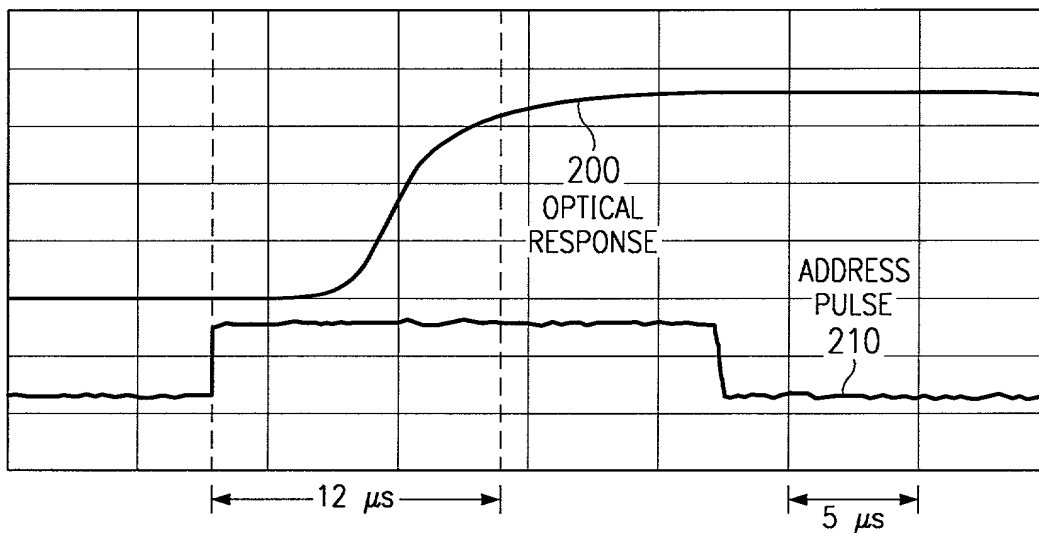
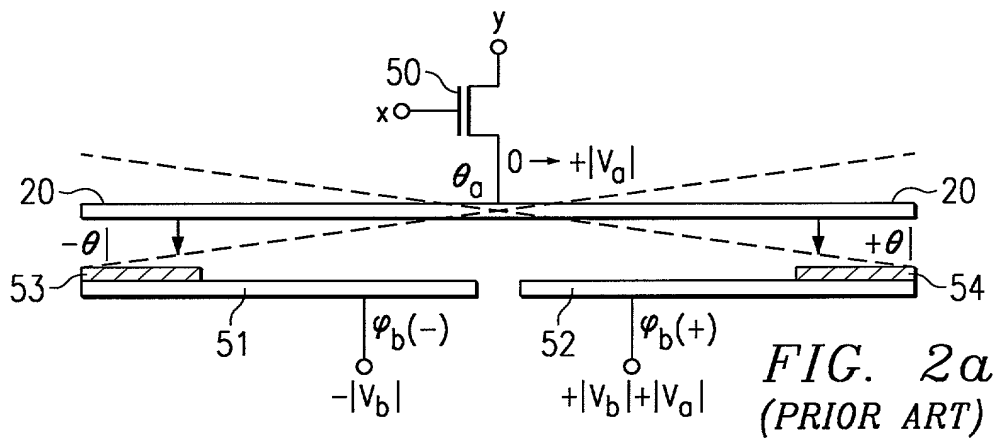
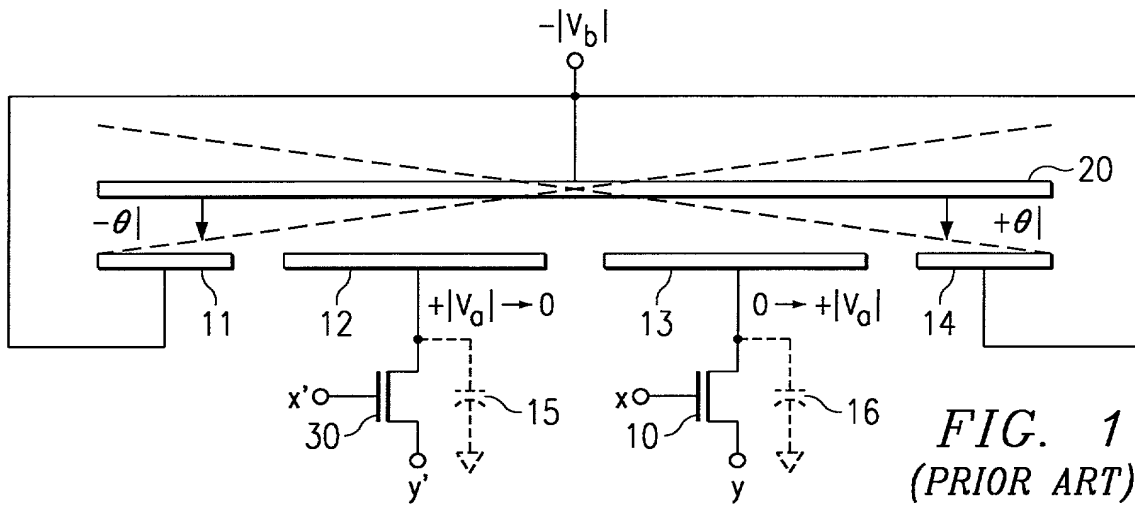
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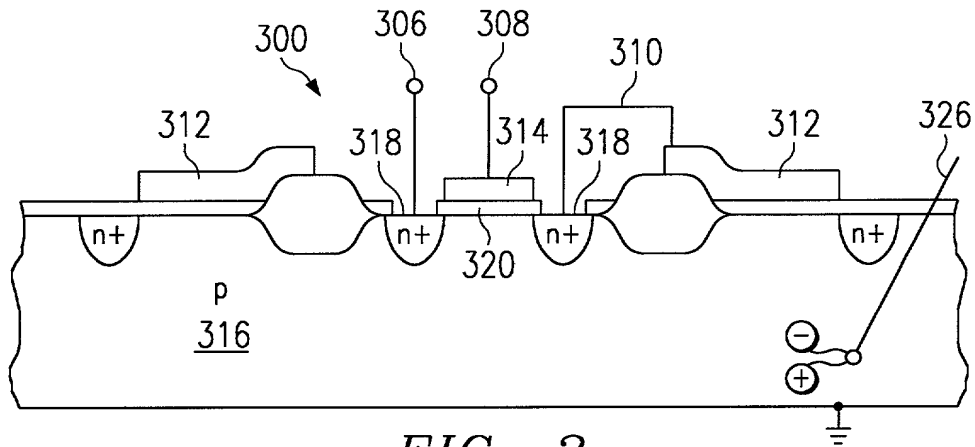


FIG. 3
(PRIOR ART)

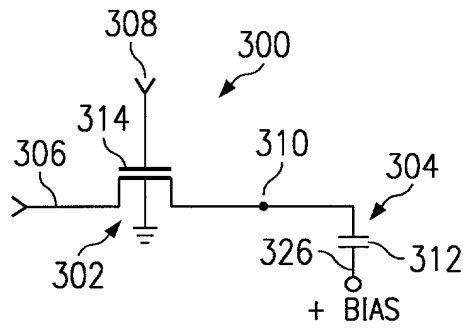


FIG. 4a
(PRIOR ART)

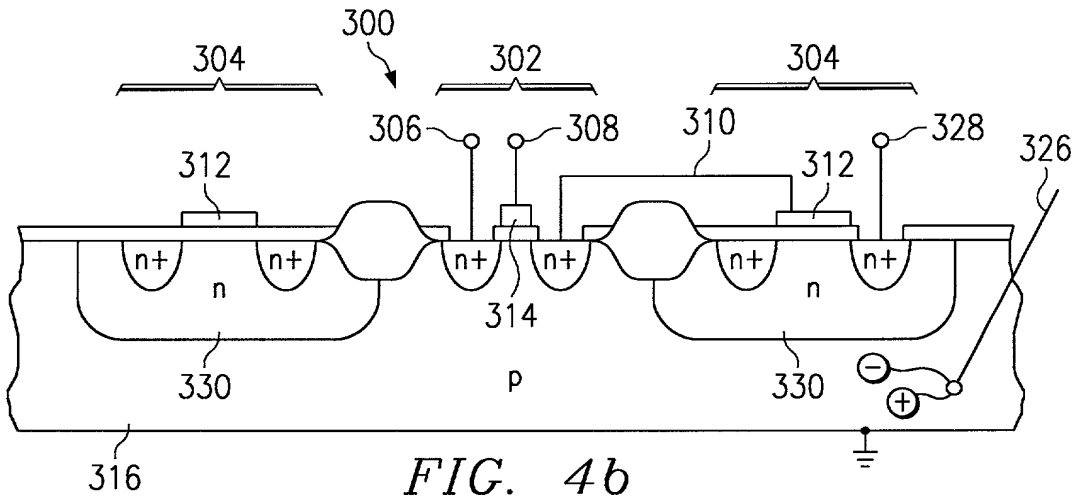


FIG. 4b
(PRIOR ART)

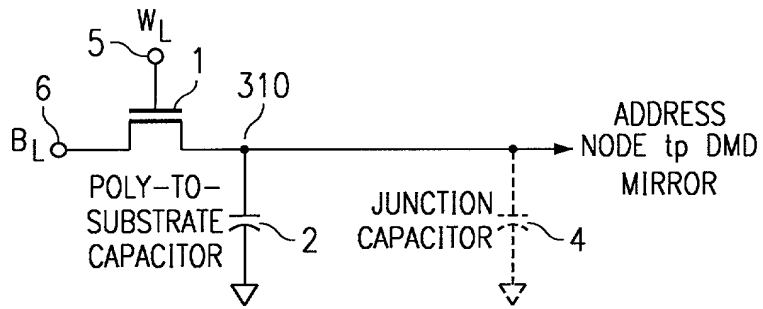


FIG. 5a

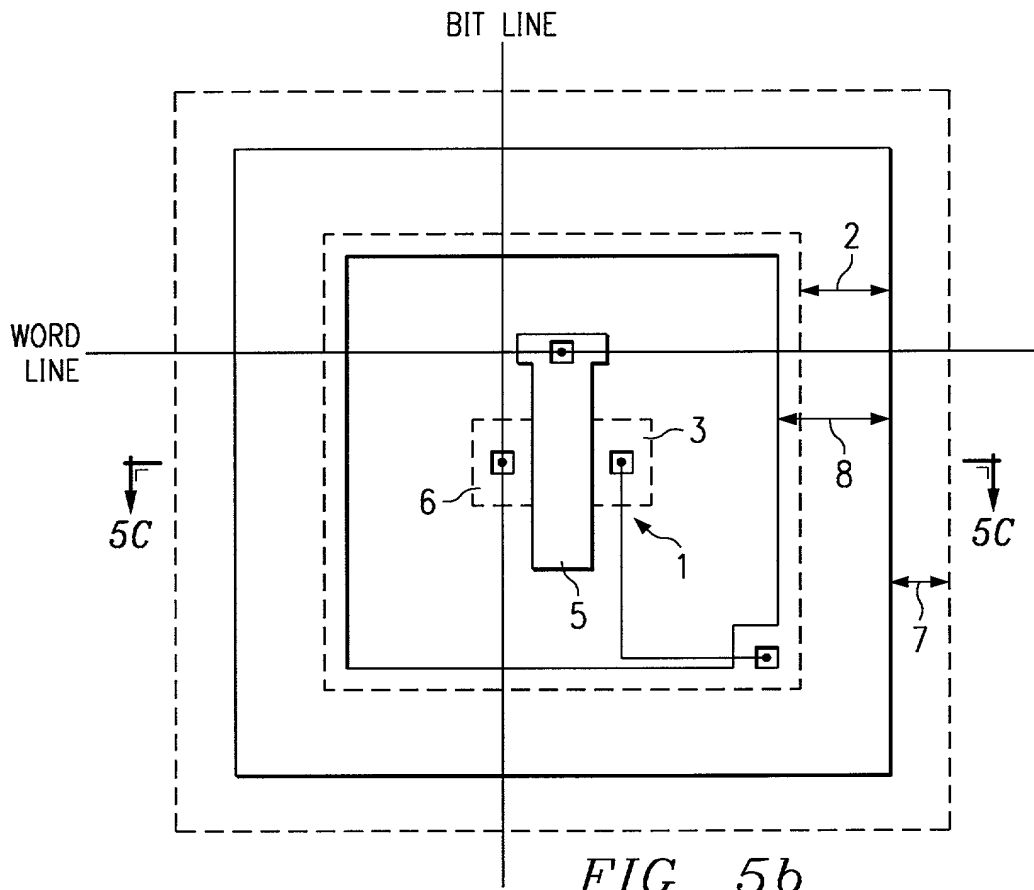


FIG. 5b

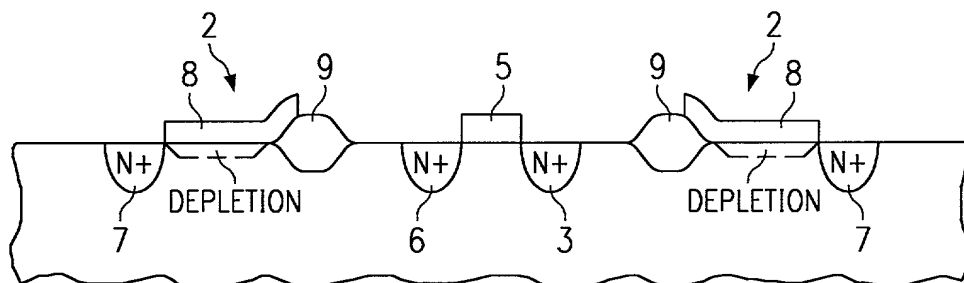
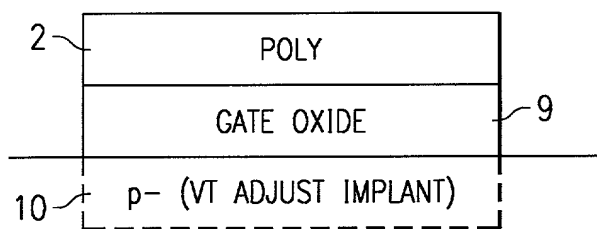


FIG. 5c



(P) FIG. 6a

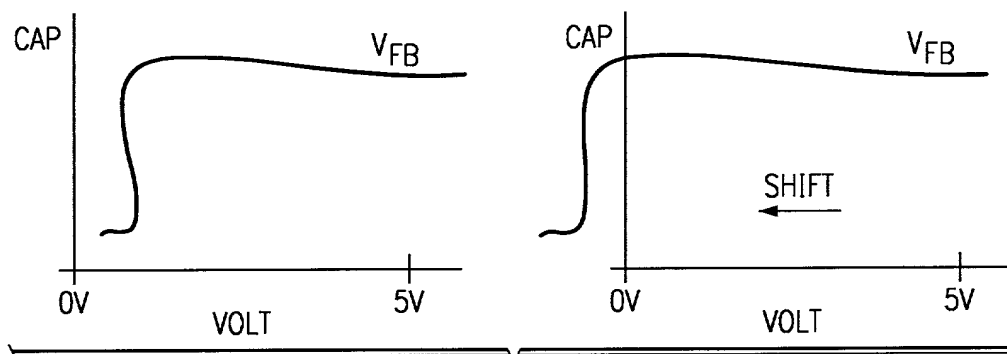


FIG. 6b

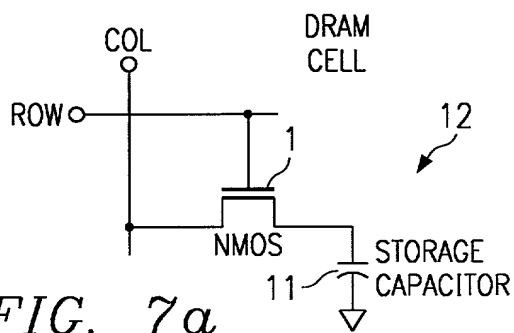


FIG. 7a

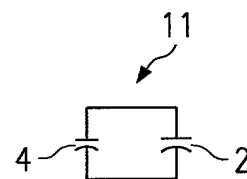


FIG. 7c

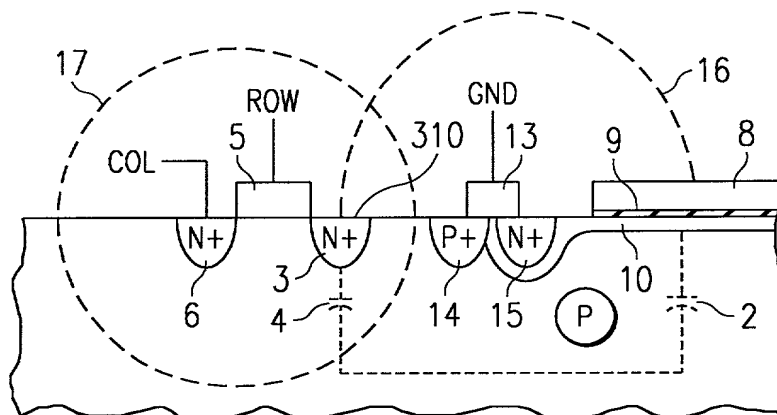
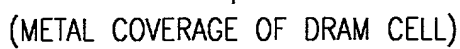
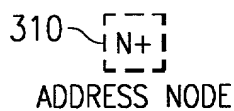


FIG. 7b

[illegible]

The timing diagram shows the voltage levels for the RESET and SET mirrors during a memory operation. The diagram is divided into two sections by a vertical dashed line. In the first section, the RESET MIRROR is at +20V, the SET MIRROR is at +5V, the RESET BAR is at -15V, and the REPLY BIAS is at 0V. In the second section, the RESET MIRROR is at -15V, the SET MIRROR is at +20V, the RESET BAR is at +20V, and the REPLY BIAS is at -15V. The labels 'RESET MIRRORS' and 'SET MIRRORS TO NEW STATE' are at the top, with arrows pointing to the RESET and SET mirror signals respectively. The labels 'APPLY BIAS' and 'REAPPLY BIAS' are also at the top, with arrows pointing to the RESET and SET mirror signals respectively.

FIG. 9b

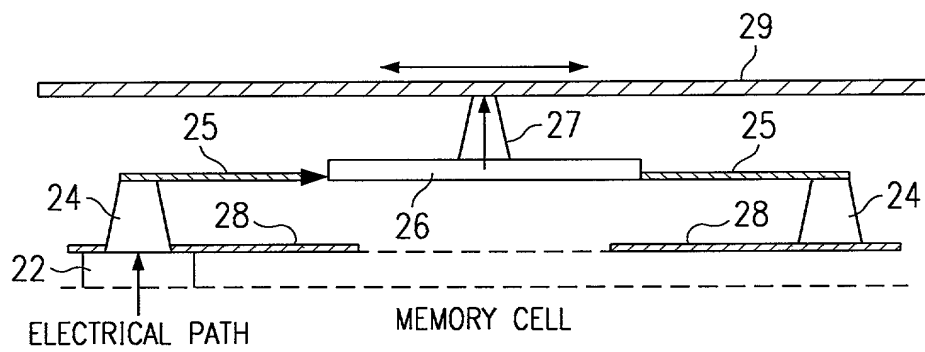
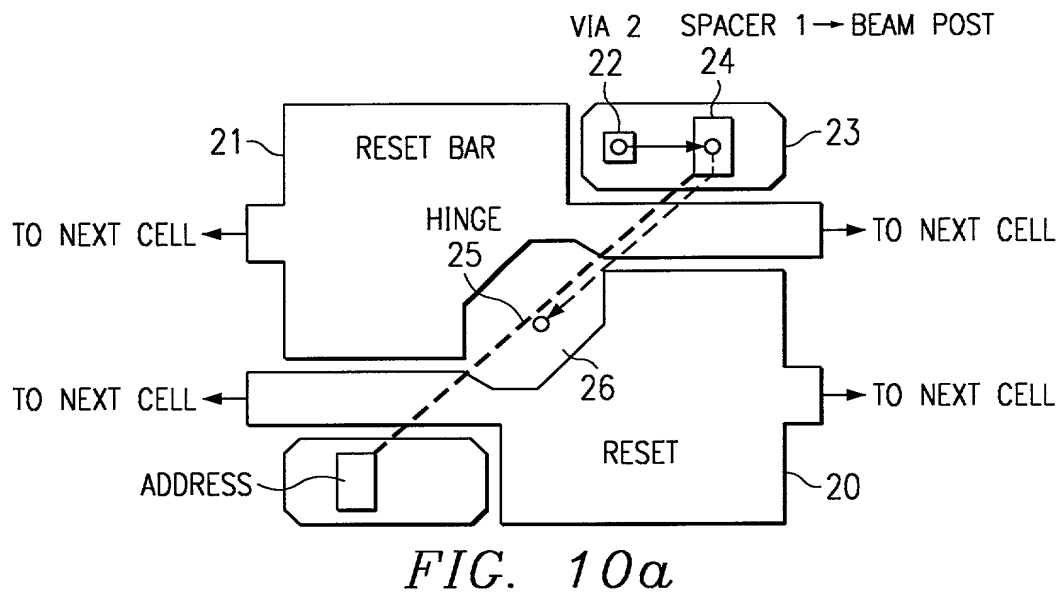
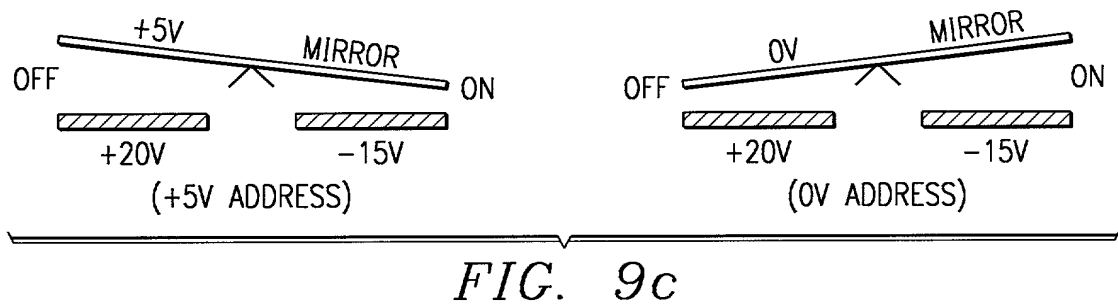


FIG. 9c

FIG. 10b

